An MMIC Low-Distortion Variable-Gain Amplifier Using Active Feedback

Kenjiro Nishikawa and Tsuneo Tokumitsu

Abstract—**A new low-distortion variable-gain amplifier (VGA) is proposed and analyzed. The VGA's gain is controlled through changing the transconductance of a common-drain FET (CDF) in the negative feedback path. The analysis and prototype results indicate that the third-order intermodulation-distortion ratio is greatly improved at high input-power levels due to a drastic reduction in the VGA's input impedance and the CDF's unilateral characteristic. The gain in a wide temperature range maintains stability due to the combination effect of the transconductances of the CDF and the amplifying FET. This CDF feedback VGA is very useful for developing a wide-dynamic range front-end MMIC. The noise and thermal performances were also measured.**

I. Introduction

VARIABLE-GAIN AMPLIFIERS (VGA's) are used in radio communication equipment to control the input-power level of mixers because the power level of the received signals varies greatly. The dynamic range of a receiver is limited at the low signal-level end by its noise figure performance and at the high signal-level end by its linearity. Recently, the maximum received-signal-level requirement has increased to a level approaching -5 to 0 dBm. This means VGA's must have a wider gain-control range and greater linearity.

Conventional VGA's utilize the gate-bias or drain-bias dependence of FET transconductance (gm) [1], [2]. Their disadvantage is that they exhibits poor linearity under compressed gain conditions. This is because FET linearity degrades as gm decreases. Another recently reported VGA is a variable-resistance negative-feedback amplifier using an FET varistor [3, 4]. The linearity of this amplifier is better than that of conventional amplifiers. The reason for this is that the varistor's impedance is decreased as the input-power level increases in order to suppress the applied voltage for amplification at the FET gate terminal. However, the minimum variable resistance is limited by the FET-varistor gate-width to about 40 Ω for a 100 μm gate FET [3], [4], and expansion of the FET gate-width degrades the VGA performance due to an increase in parasitic capacitance. Furthermore, the FET varistor is not unilateral conductivity. For these reasons, the maximum received-signal level remains limited to -10 dBm.

To solve these problems, the authors propose a new negative feedback variable-gain amplifier that utilizes a common-drain FET (CDF) in the feedback path [5]. The transconductance of the CDF controls the feedback transmission of the VGA and its variation drastically decreases the VGA input impedance, which serves to further improve the VGA's distortion characteristics. This paper presents a detailed analysis of the gain and distortion of this new VGA. In addition measured performance of a fabricated VGA is shown.

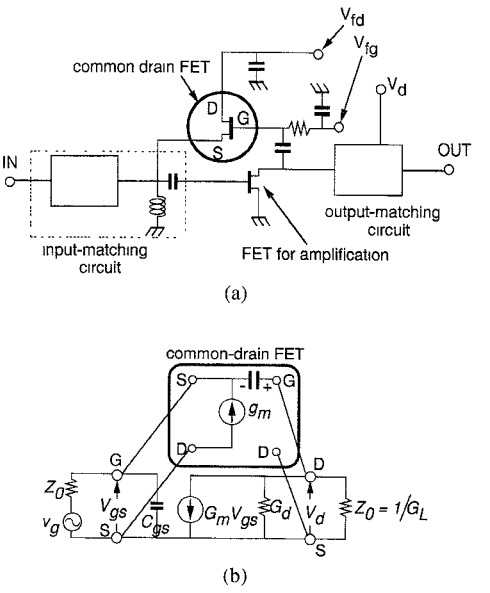

Fig. 1. Basic configuration. (a) Basic configuration of the common-drain FET feedback VGA (b) Equivalent circuit for the amplification and the feedback path.

II. Basic Theory

A. Gain Characteristic

The basic configuration of the new VGA is shown in Fig. 1(a). The VGA consists of an FET for amplification, a common-drain FET (CDF) for the feedback-path control, capacitors, and matching circuits. The CDF is connected between the drain and gate terminals of the amplifying FET through a DC-block capacitor attached to the CDF gate. The drain-current path for the CDF is served by a shunt inductance in the input-matching circuit. Fig. 1(b) shows a simplified equivalent circuit for estimating the gain-control and distortion-improvement characteristics, where Z_0, g_m, G_m, G_d and C_{gs} are the load/source impedance, the transconductance of the CDF, the transconductance, the drain conductance, and the gate source capacitance of the amplifying FET, respectively. Voltages v_g, V_{gs}, and V_d are the input voltage, the gate-source voltage, and the drain voltage, respectively.

The Y matrixes of the amplifying FET (common-source FET) and the common-drain FET in the feedback path are

$$[Y_{CSF}] = \begin{bmatrix} j\omega C_{gs} & 0 \\ G_{m0} & G_d \end{bmatrix} \quad (1)$$

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The authors are with NTT Wireless Systems Laboratories, 1-2356 Take, Yokosuka, Kanagawa 238-03, Japan.

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and

$$[Y_{\mathrm{CDF}}] = \begin{bmatrix} g_m & -g_m \\ 0 & 0 \end{bmatrix} \tag{2}$$

respectively, where G_{m0} is a linear parameter of the transconductance G_m. The two zeros in the Y matrix (2) indicate a high unilateral conductivity and a high level gate impedance in the CDF, which were confirmed through a measurement as high as 20 dB and 400 Ω for a 100 μm gate-width FET. The Y matrix of the equivalent circuit is

$$[Y] = \begin{bmatrix} j\omega C_{\mathrm{gs}} + g_m & -g_m \\ G_{m0} & G_d \end{bmatrix}. \tag{3}$$

From the Y matrix (3) amplifier gain S_{21} and input impedance Z_{in} are obtained as the following

$$S_{21} = \frac{-2G_{m0}Z_0}{1+Z_0G_d+(1+Z_0G_d+Z_0G_{m0})Z_0g_m+j\omega Z_0C_{\mathrm{gs}}(1+Z_0G_d)} \tag{4}$$

$$\approx \frac{-2G_{m0}Z_0}{1+(1+Z_0G_{m0})Z_0g_m}$$

and

$$Z_{\mathrm{in}} = \frac{1+Z_0G_d}{(1+Z_0G_d+Z_0G_{m0})g_m+j\omega C_{\mathrm{gs}}(1+Z_0G_d)} \tag{5}$$

$$\approx \frac{1}{(1+Z_0G_{m0})g_m}.$$

The above expressions show that the gain and the input impedance of the VGA can be changed by controlling the transconductance g_m of the CDF in the feedback path.

From these equations we focus on three key points.

1) VGA gain S_{21} is maximized, when the CDF is biased at the pinch-off voltage, $g_m = 0$. The dependence of the gain and input impedance on the transconductance is similar to their dependence on the variable resistance in the varistor feedback VGA.
2) VGA impedance Z_{in} is minimized when g_m is highest. It is important how low the minimum Z_{in} is, because the minimum Z_{in} is a dominant factor for increasing the level of the highest input power. Fig. 2 compares the input impedance versus gain characteristics for the CDF feedback VGA and the varistor feedback VGA. The input impedances of the CDF feedback VGA and the varistor feedback VGA decrease as the gain of those VGA's decrease, respectively. The input impedance of the CDF feedback VGA is less than that of the varistor feedback VGA over the gain range. This figure indicates that an amplifying FET in the CDF feedback VGA is maintained under a smaller signal condition than in the varistor feedback VGA under a compressed gain condition.
3) Gain variation near the minimum gain condition can be suppressed over a wide temperature range because of the decrease of the feedback signal level against the decrease of the amplifying FET's transconductance. This effect is estimated using a differential of expression (4), i.e., (4′), on the transconductance, where the variation rate of zero appears at the condition where $G_{m0}g_m = 1/Z_0^2$ and the positive variation rate at a larger g_m is strongly suppressed by the denominator including the term $(G_{m0}g_mZ_0^2)^2$.

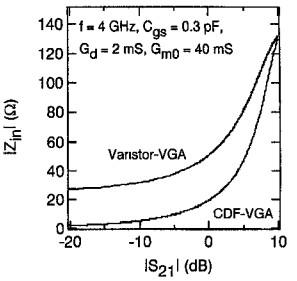


Fig. 2. Dependence of input impedance on gain.

$$\frac{\partial S_{21}}{\partial g_m} \approx \frac{-2Z_0\alpha(1-Z_0^2\alpha g_m^2)}{(1+Z_0g_m+Z_0^2\alpha g_m^2)^2} = \frac{-2Z_0\alpha(1-Z_0^2G_{m0}g_m)}{(1+Z_0g_m+Z_0^2G_{m0}g_m)^2} \tag{4′}$$

where G_{m0} is assumed to be αg_m (α is a constant).

B. Distortion Characteristic

The analysis used here is based on a power-series description [6], [7] of only the transconductance nonlinearity of the amplifying FET. The transconductance nonlinearity is principally determined using the gate-source voltage. The voltage dependence of this characteristic may be represented by a power series in the form of

$$G_m = G_{m0} + G_{m1}V_{\mathrm{gs}} + G_{m2}V_{\mathrm{gs}}^2. \tag{6}$$

From Fig. 1(b),

$$V_d = -\frac{G_m}{G_L+G_d}V_{\mathrm{gs}} = -\frac{G_{m0}V_{\mathrm{gs}} + G_{m1}V_{\mathrm{gs}}^2 + G_{m2}V_{\mathrm{gs}}^3}{G_L+G_d}. \tag{7}$$

where G_L equals $1/Z_0$. Intermodulation is defined for the case of two equal amplitude sinusoidal signals at frequencies ω_1 and ω_2. Considering the input impedance, Z_{in}, of the CDF feedback VGA, the gate bias V_{gs} is

$$V_{\mathrm{gs}} = A\, v_g(\cos(\omega_1\, t) + \cos(\omega_2\, t)) \tag{8}$$

where

$$A = \frac{Z_{\mathrm{in}}}{Z_{\mathrm{in}}+Z_0}. \tag{9}$$

The third-order intermodulation distortion ratio, D/U, is defined as the ratio of the distortion output power at $2\omega_1 - \omega_2$ to that at fundamental frequency ω_1. The D/U may be expressed as the following

$$[D/U]_{\mathrm{CDF}} = 20\log\left|\frac{V_{d\ fundamental}}{V_d 2\omega_1 - \omega_2}\right| = 20\log\left|\frac{G_{m0}Av_g + \frac{9}{4}G_{m^2}(Av_g)^3}{\frac{3}{4}G_{m2}(A\, v_g)^3}\right| \approx 20\log\left|\frac{4G_{m0}}{3G_{m2}(Av_g)^2}\right| \tag{10}$$

where $V_{d\ \mathrm{fundamental}}$ is the first-order output at the fundamental frequency ω_1, and $V_{d2\omega 1-\omega 2}$ the third-order intermodulation output at frequency $2\omega 1 - \omega 2$.

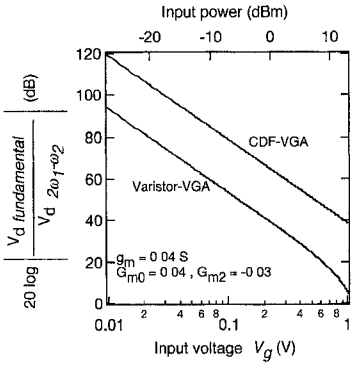


Fig. 3. D/U versus input-power voltage.

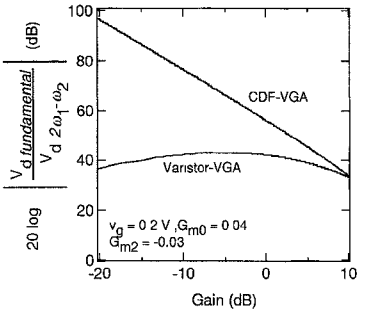


Fig. 4. D/U versus VGA gain.

The D/U of the varistor feedback VGA is obtained by utilizing the same analysis and replacing the part of the common-drain FET in Fig. 1 with a variable resistor. The D/U of the varistor feedback VGA is expressed by changing $G_{m0}Av_g$ to $(G_{m0} - 1/R_{\rm fb})Bv_g$ as in the following, where $R_{\rm fb}$ is the variable resistance and B is defined in the same manner as A

$$[D/U]_{\rm varistor} = 20\log\left|\frac{(G_{m0}-\frac{1}{R_{\rm fb}})Bv_g + \frac{9}{4}G_{m2}(Bv_g)^3}{\frac{3}{4}G_{m2}(Bv_g)^3}\right| \approx 20\log\left|\frac{4(G_{m0}-\frac{1}{R_{\rm fb}})}{3G_{m2}(Bv_g)^2}\right|. \quad (11)$$

For both expressions (10) and (11), Av_g and Bv_g are maintained as constant or degrade as v_g increase. Av_g is lower than Bv_g as seen from Fig. 2; therefore, $[D/U]_{\rm CDF}$ is considered to be higher than $[D/U]_{\rm varistor}$ at each input-power level. Furthermore, expression (11) has a part, $G_{m0} - 1/R_{\rm fb}$, that degrades its value as v_g increases while the corresponding part, G_{m0}, in expression (10) is constant. This constant value is due to the unilateral characteristic of the CDF described by expression (2). These effects expand the difference in D/U between the CDF feedback VGA and the varistor feedback VGA at the lower gain, i.e., at the higher input power level.

Fig. 3 compares the dependence of D/U on the input power, v_g, for the CDF feedback VGA and the varistor feedback VGA at the minimum gain, $g_m = 0.04$ S. The curves are calculated using the above expressions. The results indicate an input-power level improvement of as large as 10 dB. Fig. 4 compares the D/U versus gain characteristics of the VGA's under a gain-control condition where an input-power level of $v_g = 0.2$ V is kept constant (nearly 0 dBm). As predicted, the CDF feedback VGA provides much higher linearity at high input powers and lower gain than the varistor feedback VGA. The D/U of the CDF feedback VGA increases linearly as the gain decreases, while that of the varistor feedback VGA does not.

III. Fabrication and Measured Results

A. Circuit Design

Fig. 5 shows the circuit schematic of a fabricated 4 GHz CDF feedback VGA. This VGA uses a cascode-FET for a higher gain against the parasitic effects of the CDF in the feedback path. The CDF is connected between the cascode FET's

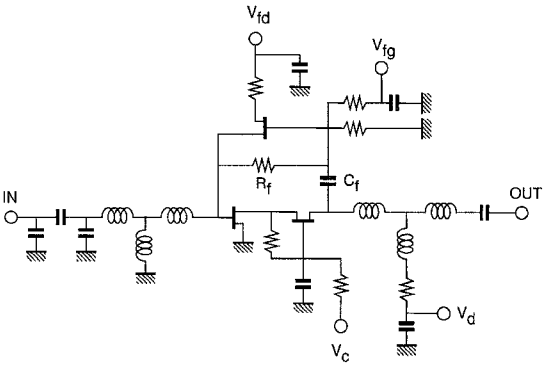


Fig. 5. Circuit schematic of a fabricated 4 GHz CDF feedback VGA.

drain and gate via a DC-block capacitor C_f. The resistor R_f in the feedback path is used to stabilize the highest-gain operation. The impedance matching circuits are designed to provide a small signal gain of 7 dB from 3 GHz to 4.5 GHz. $V_{\rm fg}$ and $V_{\rm fd}$ are the gate bias and the drain bias for the CDF, respectively, and are used to control VGA gain. V_d and V_c are the drain bias and the second gate bias for the cascode-FET, respectively. The gate bias for the cascode-FET is constant at 0 V.

The FET used in this VGA is a 0.3 μm gate-length MESFET with a transconductance of 200 mS/mm and a gate source capacitance of 4 pF/mm at a $V_{\rm ds}$ of 3 V and a $V_{\rm gs}$ of 0 V. The gate width of both FET's was determined so as to minimize the minimum gain variation over a wide temperature range according to expression (4′) and also to attain a reasonable gain. The stability factor K on the gate-source capacitance of the CDF was also considered in the VGA design because a larger gate-width FET offers lower K value. As a result, the gate width of 200 μm was selected.

B. Variable Gain Performance

A micro-photograph of a 4 GHz CDF feedback VGA is shown in Fig. 6. The chip size is 1.41 mm × 1.43 mm. The pattern layout was performed based on the uniplaner MMIC and minimized the feedback path length.

Fig. 7 shows the measured variable-gain performance of the VGA. The black lines represent the measured results and the gray line represents the simulation. The gain is controlled by varying V_{fg}, that is the gate bias for the CDF. V_d, V_c, and V_{fd} are constant at 5 V, 2.5 V, and 3 V, respectively. The gain varies more than 15 dB in the 3 to 4.5 GHz frequency range, over the gain-control voltage, V_{fg}, from −7 to 0 V. A three-stage VGA provides a sufficient gain-control range for

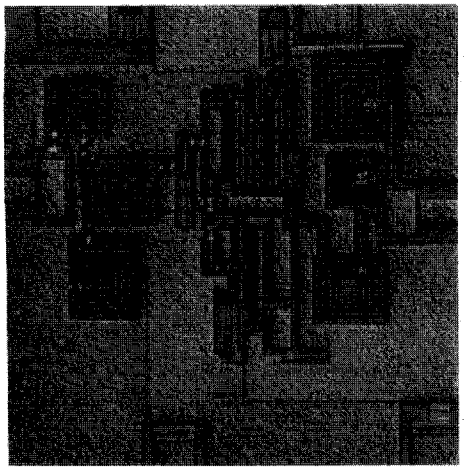


Fig. 6. Micro-photograph of a 4-GHz CDF feedback VGA. Chip size is 1.41 mm × 1.43 mm.

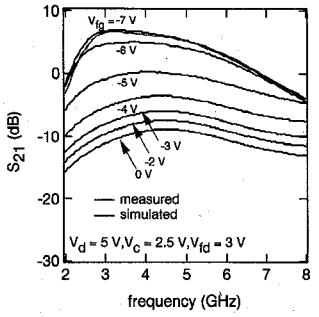


Fig. 7. Variable gain performance.

digital radio systems [4]. The output return loss variation is less than 3.5 dB peak-to-peak over the gain-control range. The input return loss decreases as the control voltage varies from −7 to 0 V due to the input impedance control for a linear operation. The input impedance change can be masked using a front-end low-noise amplifier.

The noise figure performance of the CDF feedback VGA is shown in Fig. 8. Gray lines represent the noise figure and the black lines represent the gain. The noise figure is 7 dB at the maximum gain, and 17 dB at the minimum gain. The noise figure increase is within 10 dB while the gain suppression is over 15 dB. These performance levels are roughly the same as those of the varistor feedback VGA.

C. Intermodulation Distortion Improvement

Fig. 9 compares the D/U versus input power characteristics on the compressed gain operation, for the CDF feedback VGA and the varistor feedback VGA. The varistor feedback VGA is designed to have similar gain-frequency characteristics. The D/U of the CDF feedback VGA is 15 dB higher than that of the varistor feedback VGA. The input power improvement is more than 8 dB at a D/U of 50 dB. A D/U of over 50 dB represents linear operation for a microwave system. The above result indicates that the CDF feedback VGA provides linear variable-gain amplification to an input-power level of 0 dBm.

Fig. 10 shows the linearity of the CDF feedback VGA at various control voltages. Closed circles indicate the maximum input power satisfying a D/U of 50 dB and the open circles

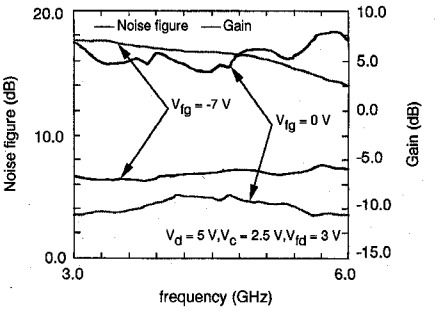


Fig. 8. Noise figure performance.

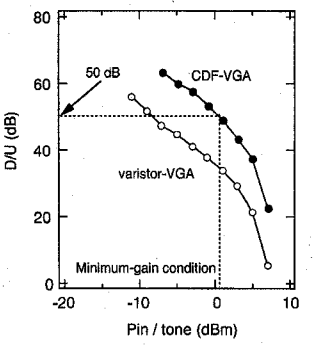


Fig. 9. Measured distortion performance. Comparison between CDF feedback VGA and varistor feedback VGA.

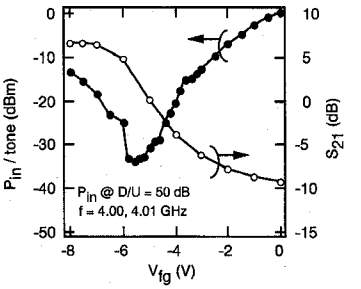


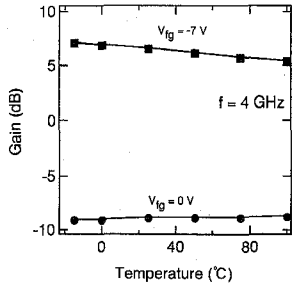
Fig. 10. Maximum input power and associated gain of the CDF feedback VGA over control voltages between −8 V and 0 V.

show the corresponding amplifier gain. The region under the D/U curve indicates linear operation (D/U > 50 dB). The maximum input power increases at V_{fg} from −5.8 V to 0 V although it degrades at V_{fg} from −8 V to −5.8 V. The maximum input power at the minimum gain is distinctly higher than that at the maximum gain. Such significant improvement is not possible with conventional VGA's.

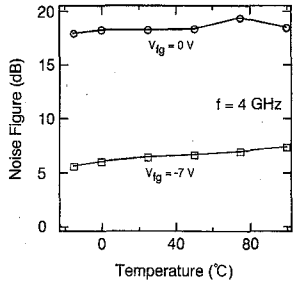
The above measured results of the CDF feedback VGA exhibit great linearity and confirm the analysis.

D. Thermal Stability

Fig. 11 shows the thermal performance of the VGA gain and noise figure. Fig. 11(a) shows the gain and Fig. 11(b) shows the noise figure. In Fig. 11 the square marks indicate performance at the maximum gain and the circle marks show that at the minimum gain. The maximum gain varies 2 dB at the frequency of 4 GHz from −15°C to 100°C, while the minimum gain is constant. The noise figure varies less than 2 dB at the maximum and minimum gain value. The measured D/Us on the minimum gain condition at −15°C and 100°C



(a)



(b)

Fig. 11. Thermal performance of VGA gain and noise figure. (a) Thermal performance of VGA gain. (b) Thermal performance of VGA noise figure.

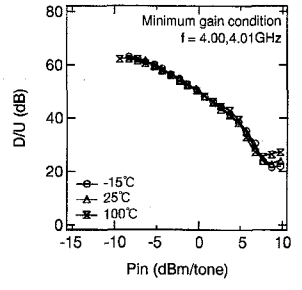


Fig. 12. Thermal performance of D/U.

are compared with that of 25°C in Fig. 12. The maximum input powers needed to achieve a D/U of 50 dB at −15°C, 25°C, and 100°C are nearly the same. These results indicate that this VGA offers highly stable distortion performance over a wide temperature range. The reason is considered to be that the transconductances of the cascode FET and the CDF decrease at the same rate as the temperature increases.

IV. Conclusion

A common-drain FET feedback variable-gain amplifier was proposed, analyzed and demonstrated. VGA gain is controlled using the transconductance of the CDF placed in the feedback path. An analysis indicates that the third-order intermodulation distortion ratio of the CDF feedback VGA is drastically improved due to the reduction in the VGA's input impedance and the unilateral conductivity of the CDF. The measured data confirm that the CDF feedback VGA has higher linearity under compressed gain conditions than do conventional VGA's. Furthermore, the thermal stability of the VGA under compressed gain operation retains its high level of performance in a wide temperature range between −15°C and 100°C.

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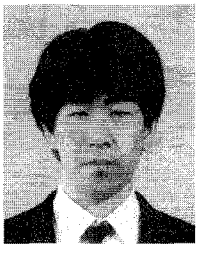
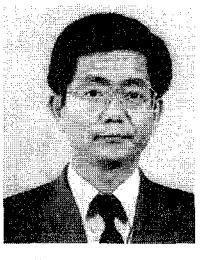


Kenjiro Nishikawa was born in Nara, Japan, on September 18, 1965. He received the B.E. and M.E. degrees in welding engineering from Osaka University, Suita, Japan, in 1989 and 1991, respectively.

In 1991, he joined the NTT Radio Communication Systems Laboratories (now NTT Wireless Systems Laboratories), Yokosuka, Japan. He has been engaged in research and development on highly integrated MMIC's (monolithic microwave integrated circuits), such as one chip receiver and in research on three-dimensional MMIC's.

Dr. Nishikawa is a member of Institute of Electronics, Information and Communication Engineering (IEICE) of Japan and IEEE.



Tsuneo Tokumitsu was born in Hiroshima, Japan, in 1952. He received the B.S. and M.S. degrees in electronics engineering from Hiroshima University, Hiroshima, Japan, in 1974 and 1976, respectively.

He joined the Yokosuka Electrical Communication Laboratories, Nippon Telegraph and Telephone Public Corporation (NTT), Yokosuka, Japan, in 1976. He had been involved in developmental research on microwave and millimeter-wave GaAs FET circuits and GaAs MMIC's for space applications. In 1986, he jointed ATR Optical and Radio Communications Research Laboratories, Osaka (now Kyoto), Japan, on leave from NTT. At ATR his primary interests were in achieving FET-sized, wide-band circuit function modules (LUFET's), multilayer MMIC's, and active inductors for highly integrated MMIC's. Since Feb. 1990, he has been with NTT Radio Communication Systems Laboratories, Yokosuka, Japan. After the accomplished high-linearity MMIC T/R modules for 16-QAM digital radio trunk transmission systems in early 1993, he has been engaged in developmental research on novel MMIC technology including three-dimensional and advanced uniplanar MMIC's.

Mr. Tokumitsu is a recipient each of the 1991 Microwave Prize granted by the IEEE MTT Society, the Ichimura Prizes in Technology—Meritorious Achievement Prize granted in 1994 by the New Technology Development (Ichimura) Foundation. He is a member of the Institute of Electronics, Information and Communication Engineering of Japan.